DATA SHEET

P89LPC913

80C51 8-bit microcontroller with two-clock core

1 KB 3 V low-power Flash with 128 Byte RAM

Preliminary data

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Philips
Semiconductors

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GENERAL DESCRIPTION

The P89LPC913 is a single-chip microcontroller designed for applications demanding high-integration, low cost solutions over a wide range of performance requirements. The P89LPC913 is based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system level functions have been incorporated into the P89LPC913 in order to reduce component count, board space, and system cost.

FEATURES

- A high performance 80C51 CPU provides instruction cycle times of 167-333 ns for all instructions except multiply and divide when executing at 12 MHz. This is 6 times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 1 KB Flash code memory with 256 byte erasable sectors and 16-byte erasable page size.
- 128-byte RAM data memory.
- Serial Flash In-Circuit Programming (ICP) allows simple production coding with commercial eprom programmers. Flash security bits prevent reading of sensitive application programs.
- In-Application Programming (IAP) and byte erase allows code memory to be used for non-volatile data storage.
- Two 16-bit counter/timers. Each timer may be configured to toggle a port output upon timer overflow or to become a PWM output.
- Real-Time clock that can also be used as a system timer.
- Two analog comparators with selectable inputs and reference source.
- Enhanced UART with fractional baudrate generator, break detect, framing error detection, automatic address detection and versatile interrupt capabilities.
- SPI communication port.
- Four keypad interrupt inputs.
- Four interrupt priority levels.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from 8 values.
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Low voltage reset (Brownout detect) allows a graceful system shut-down when power fails. May optionally be configured as an interrupt.
- Oscillator Fail Detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Configurable on-chip oscillator with frequency range options selected by user programmed Flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 12 MHz.
- Internal RC oscillator option allows operation without external oscillator components.The RC oscillator option is selectable and fine tunable.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port "input pattern match" detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Second data pointer.
- Schmitt trigger port inputs.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- 9 I/O pins minimum. Up to 12 I/O pins when using internal oscillator and reset options.
- Only power and ground connections are required to operate the P89LPC913 when internal reset option is selected.
- Serial Flash programming allows simple in-circuit production coding. Flash security bits prevent reading of sensitive application programs.
- In-Application Programming of the Flash code memory. This allows changing the code in a running application.

- Idle and two different Power down reduced power modes. Improved wakeup from Power down mode (a low interrupt input starts execution). Typical Power down current is 1µA (total Power down with voltage comparators disabled).
- 14-pin TSSOP and DIP packages.
- Emulation support.

ORDERING INFORMATION

Part Number	Package	Temperature Range	Frequency	Drawing Number
P89LPC913BA	DIP 14	0 to +70 °C	0-12 MHz	
P89LPC913BDH	TSSOP14	0 to +70 °C	0-12 MHz	

LOGIC SYMBOL

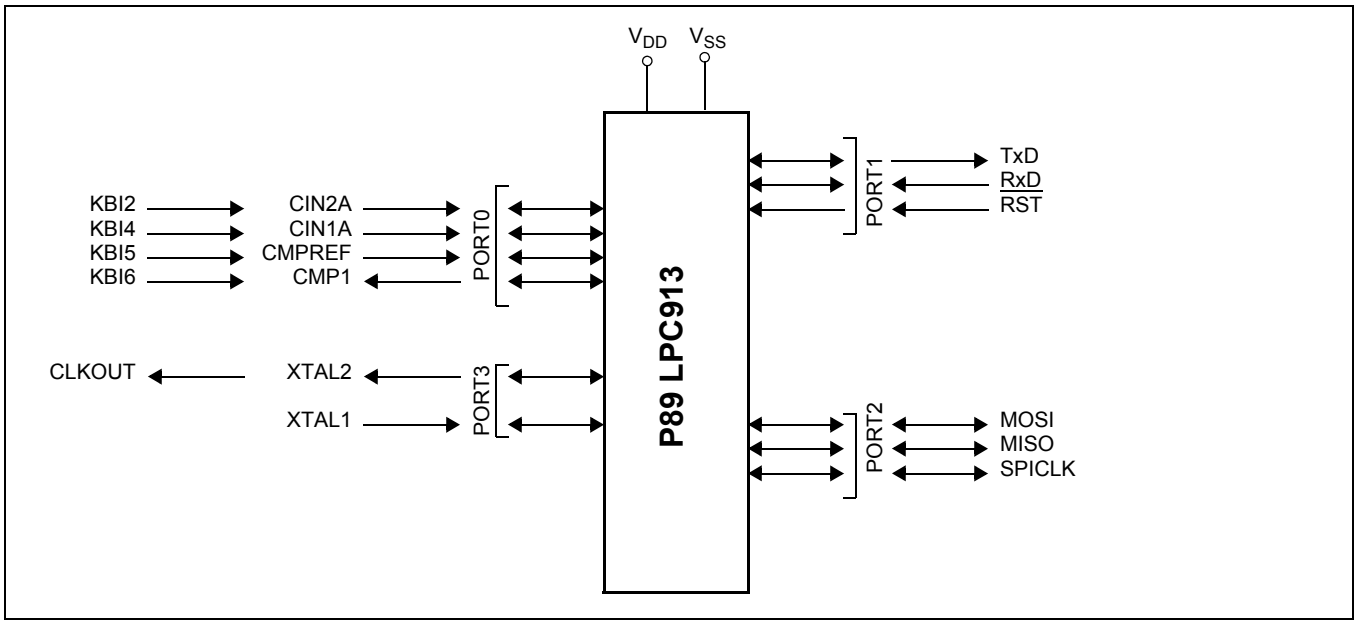


Figure 1: Logic symbol.

BLOCK DIAGRAM

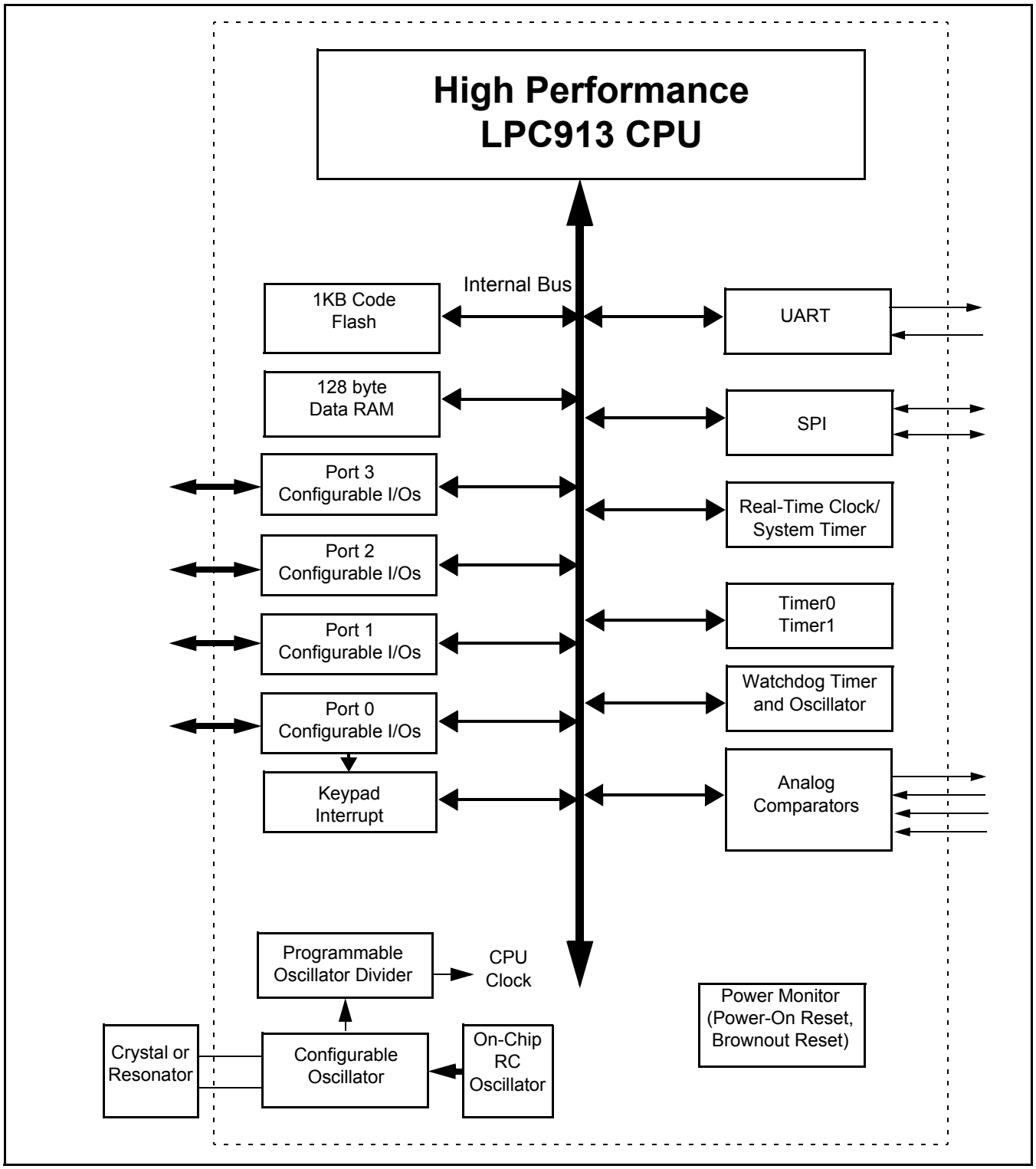
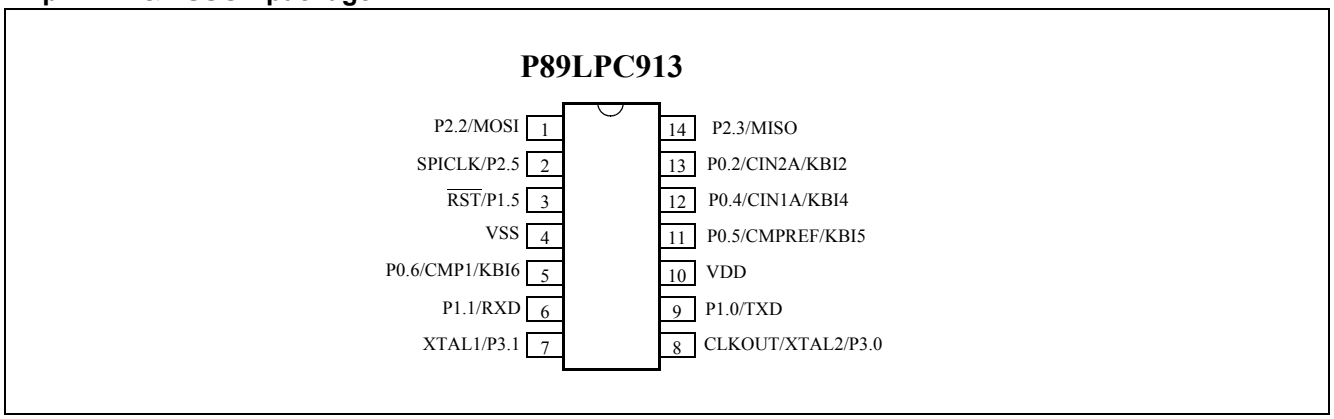


Figure 2: Block diagram.

PIN CONFIGURATION

14-pin DIP & TSSOP package



PIN DESCRIPTIONS

MNEMONIC	PIN NO. for TSSOP14/ DIP14	TYPE	NAME AND FUNCTION
P0.2, P0.4 - P0.6	5, 11, 12, 13	I/O	**Port 0:** Port 0 is an 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pullup disabled. The operation of port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. The Keypad Interrupt feature operates with port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below.
	13	I/O I I	**P0.2** Port 0 bit 2. **CIN2A** Comparator 2 positive input A. **KBI2** Keyboard Input 2.
	12	I/O I I	**P0.4** Port 0 bit 4. **CIN1A** Comparator 1 positive input A. **KBI4** Keyboard Input 4.
	11	I/O I I	**P0.5** Port 0 bit 5. **CMPREF** Comparator reference (negative) input. **KBI5** Keyboard Input 5.
	5	I/O O I	**P0.6** Port 0 bit 6. **CMP1** Comparator 1 output. **KBI6** Keyboard Input 6.
P1.0, P1.1, P1.5	3,6,9	I/O(P1.0, P1.1,); I (P1.5)	**Port 1:** Port 1 is an 3-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pullup disabled. The operation of the configurable port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below.
	9	I/O O	**P1.0** Port 1 bit 0. **TxD** Transmitter output for the serial port.
	6	I/O I	**P1.1** Port 1 bit 1. **RxD** Receiver input for the serial port.
	3	I I	**$\overline{\text{P1.5}}$** Port 1 bit 5. (Input only) **RST** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input a low on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force In-System Programming mode.
P2.2, P2.3, P2.5	13,14,16	I/O	**Port 2:** Port 2 is a 3-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pullup disabled. The operation of port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below.

MNEMONIC	PIN NO. for TSSOP14/ DIP14	TYPE	NAME AND FUNCTION
	13	I/O	**P2.2** Port 2 bit 2.
		I/O	**MOSI** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
	14	I/O	**P2.3** Port 2 bit 3.
		I/O	**MISO** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
	16	I/O	**P2.5** Port 2 bit 5.
		I/O	**SPICLK** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 - P3.1	7,8	I/O	**Port 3:** Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pullup disabled. The operation of port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	8	I/O	**P3.0** Port 3 bit 0.
		O	**XTAL2** Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration).
		O	**CLKOUT**CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
	7	I/O	**P3.1** Port 3 bit 1.
		I	**XTAL1** Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, AND if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/ system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power down modes.

SPECIAL FUNCTION REGISTERS

Note: Special Function Registers (SFRs) accesses are restricted in the following ways:

1. User must NOT attempt to access any SFR locations not defined.
2. Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
3. SFR bits labeled '-', '0' or '1' can ONLY be written and read as follows:
   - '-' Unless otherwise specified, MUST be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
   - '0' MUST be written with '0', and will return a '0' when read.
   - '1' MUST be written with '1', and will return a '1' when read.

SPECIAL FUNCTION REGISTERS TABLE

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value Hex	Reset Value Binary
			E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00H	00000000
AUXR1#	Auxiliary Function Register	A2H	CLKLP	EBRR	-	-	SRST	0	-	DPS	00H[1]	000000x0
			F7	F6	F5	F4	F3	F2	F1	F0		
B*	B Register	F0H									00H	00000000
BRGR0#§	Baud Rate Generator Rate Low	BEH									00H	00000000
BRGR1#§	Baud Rate Generator Rate High	BFH									00H	00000000
BRGCON#	Baud Rate Generator Control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00H[%]	xxxxxx00
CMP1#	Comparator 1 Control Register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00H[1]	xx000000
CMP2#	Comparator 2 Control Register	ADH	-	-	CE2	-	CN2	-	-	CMF2	00H[1]	xx000000
DIVM#	CPU Clock Divide-by-M Control	95H									00H	00000000
DPTR	Data Pointer (2 bytes)											
DPH	Data Pointer High	83H									00H	00000000
DPL	Data Pointer Low	82H									00H	00000000
FMADRH#	Program Flash Address High	E7H	-	-	-	-	-	-			00H	00000000
FMADRL#	Program Flash Address Low	E6H									00H	00000000
FMCON#	Program Flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70H	01110000
	Program Flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA#	Program Flash Data	E5H									00H	00000000
			AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt Enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00H	00000000
			EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*#	Interrupt Enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	-	00H[1]	00x00000
			BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt Priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00H[1]	x0000000
IP0H#	Interrupt Priority 0 High	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00H[1]	x0000000
			FF	FE	FD	FC	FB	FA	F9	F8		

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value Hex	Binary
IP1*#	Interrupt Priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	-	00H[1]	00x00000
IP1H#	Interrupt Priority 1 High	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	-	00H[1]	00x00000
KBCON#	Keypad Control Register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00H[1]	xxxxxx00
KBMASK#	Keypad Interrupt Mask Register	86H									00H	00000000
KBPATN#	Keypad Pattern Register	93H									FFH	11111111
			87	86	85	84	83	82	81	80		
P0*	Port 0	80H		CMP1/ KB6	CMPREF/ KB5	CIN1A/ KB4		CIN2A/ KB2			Note 1	
			97	96	95	94	93	92	91	90		
P1*	Port 1	90H			$\overline{RST}$				RxD	TxD	Note 1	
			A7	A6	A5	A4	A3	A2	A1	A0		
P2*	Port 2	A0H			SPICLK		MISO	MOSI			Note 1	
			B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H							XTAL1	XTAL2	Note 1	
P0M1#	Port 0 Output Mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)			FFH	11111111
P0M2#	Port 0 Output Mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)			00H	00000000
P1M1#	Port 1 Output Mode 1	91H			-				(P1M1.1)	(P1M1.0)	D3H[1]	11x1xx11
P1M2#	Port 1 Output Mode 2	92H			-				(P1M2.1)	(P1M2.0)	00H[1]	00x0xx00
P2M1#	Port 2 Output Mode 1	A4H			(P2M1.5)		(P2M1.3)	(P2M1.2)			FFH	11111111
P2M2#	Port 2 Output Mode 2	A5H			(P2M2.5)		(P2M2.3)	(P2M2.2)			00H	00000000
P3M1#	Port 3 Output Mode 1	B1H							(P3M1.1)	(P3M1.0)	03H[1]	xxxxxx11
P3M2#	Port 3 Output Mode 2	B2H							(P3M2.1)	(P3M2.0)	00H[1]	xxxxxx00
PCON#	Power Control Register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00H	00000000
PCONA#	Power Control Register A	B5H	RTCPD	-	VCPD	-	-	SPPD	SPD	-	00H[1]	00000000
			D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program Status Wword	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H	00000000
PT0AD#	Port 0 Digital Input Disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00H	xx00000x
RSTSRC#	Reset Source Register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	Note 2	
RTCCON#	Real-Time Clock Control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60H[1,5]	011xxx00
RTCH#	Real-Time Clock Register High	D2H									00H[5]	00000000
RTCL#	Real-Time Clock Register Low	D3H									00H[5]	00000000

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value Hex	Binary
SADDR#	Serial Port Address Register	A9H									00H	00000000
SADEN#	Serial Port Address Enable	B9H									00H	00000000
SBUF	Serial Port Data Buffer Register	99H									xxH	xxxxxxxx
			9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H	00000000
SSTAT#	Serial Port Extended Status Register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00H	00000000
SP	Stack Pointer	81H									07H	00000111
SPCTL#	SPI Control Register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04H	00000100
SPSTAT#	SPI Status Register	E1H	SPIF	WCOL	-	-	-	-	-	-	00H	00xxxxxx
SPDAT#	SPI Data Register	E3H									00H	00000000
			8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 Control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00H	00000000
TH0	Timer 0 High	8CH									00H	00000000
TH1	Timer 1 High	8DH									00H	00000000
TL0	Timer 0 Low	8AH									00H	00000000
TL1	Timer 1 Low	8BH									00H	00000000
TMOD	Timer 0 and 1 Mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00H	00000000
TRIM#	Internal Oscillator Trim Register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	Notes 4,5	
WDCON#	Watchdog Control Register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	Notes 3,5	
WDL#	Watchdog Load	C1H									FFH	11111111
WFEED1#	Watchdog Feed 1	C2H										
WFEED2#	Watchdog Feed 2	C3H										

Notes:

* SFRs are bit addressable.

\# SFRs are modified from or added to the 80C51 SFRs.

\- Reserved bits, must be written with 0's.

§ BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any of them is written if BRGEN = 1, result is unpredictable.

Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

1. All ports are in input only (high impendance) state after power-up.
2. The RSTSRC register reflects the cause of the P89LPC913 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF - the power-on reset value is xx110000.
3. After reset, the value is 111001x1, i.e., PRE2-PRE0 are all 1, WDRUN=1 and WDCLK=1. WDTOF bit is 1 after watchdog reset and is 0 after power-on reset. Other resets will not affect WDTOF.
4. On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.
5. The only reset source that affects these SFRs is power-on reset.

FUNCTIONAL DESCRIPTION

(Please refer to the P89LPC913 User's Manual for a more detailed functional description).

ENHANCED CPU

The P89LPC913 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

CLOCKS

Clock Definitions

The P89LPC913 device has several internal clocks as defined below:

- OSCCLK - Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 3) and can also be optionally divided to a slower frequency (see section "CPU Clock (CCLK) Modification: DIVM Register"). **Note**: f_{OSC} is defined as the OSCCLK frequency.
- CCLK - CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).).
- RCCLK - The internal 7.373 MHz RC oscillator output.
- PCLK - Clock for the various peripheral devices and is CCLK/2

CPU Clock (OSCCLK)

The LPC913 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

Low Speed Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

Medium Speed Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

High Speed Oscillator Option

This option supports an external crystal in the range of 4 MHz to 12 MHz. Ceramic resonators are also supported in this configuration.

Clock Output

The LPC913 supports a user selectable clock output function on the XTAL2 / CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the Real-Time clock is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the LPC913. This output is enabled by the ENCLK bit in the TRIM register

The frequency of this clock output is $^1/_2$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

ON-CHIP RC OSCILLATOR OPTION

The P89LPC913 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ±2.5%. End user applications can write to the Trim register to adjust the on-chip RC oscillator to other frequencies.

WATCHDOG OSCILLATOR OPTION

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

EXTERNAL CLOCK INPUT OPTION

In this configuration, the processor clock is derived from an external source driving the XTAL1 / P3.1 pin. The rate may be from 0 Hz up to 12 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output.

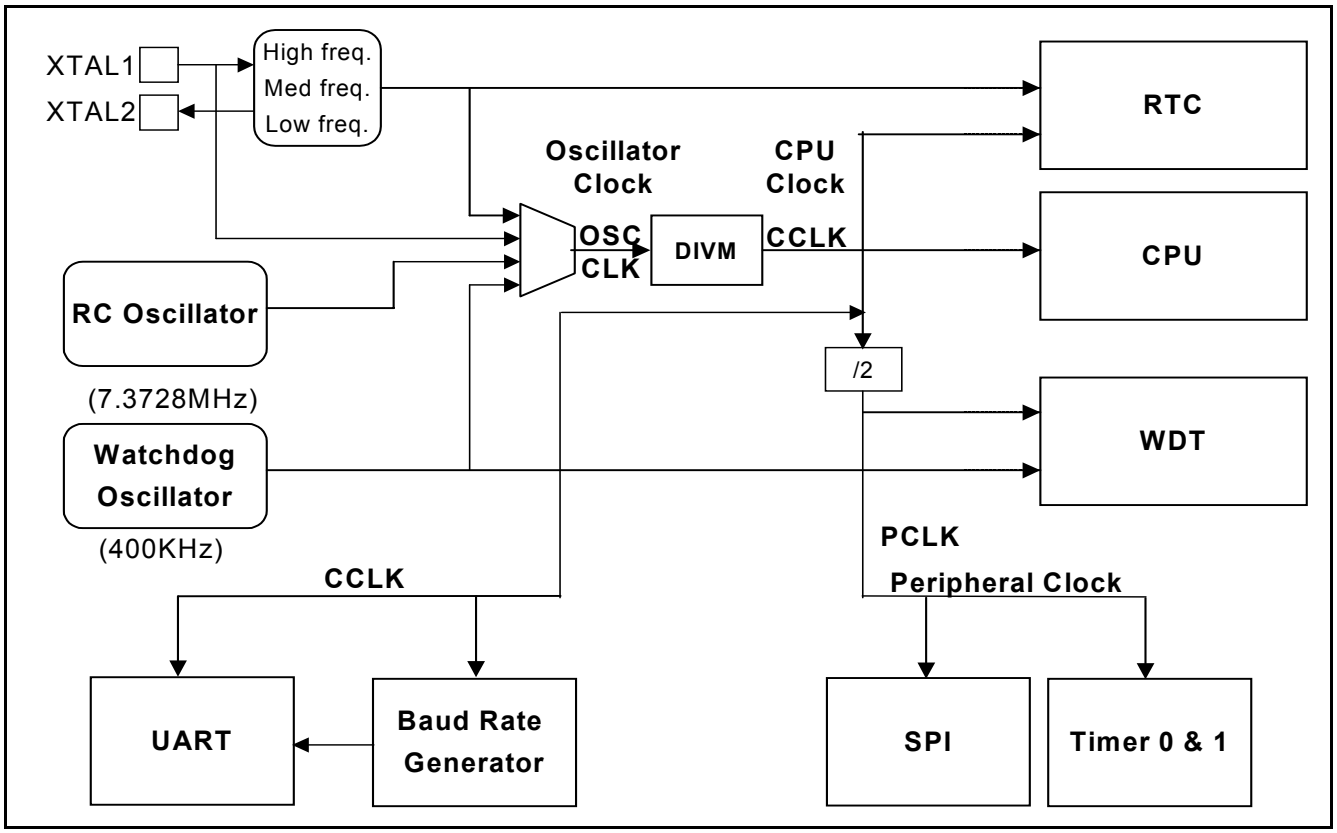


Figure 3: Block diagram of LPC913 oscillator control

CPU CLOCK (CCLK) WAKEUP DELAY

- The LPC913 has an internal wakeup timer that delays the clock until it stabilizes, depending to the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60-100 µs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60-100 µs

CPU CLOCK (CCLK) MODIFICATION: DIVM REGISTER

The OSCCLK frequency can be divided down up to 256 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

LOW POWER SELECT

The P89LPC913 is designed to run at 12 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ’1’ to lower the power consumption further. On any reset, CLKLP is ’0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

MEMORY ORGANIZATION

The various P89LPC913 memory spaces are as follows:

DATA 128 bytes of internal data memory space (00h..7Fh) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

SFR Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

CODE 64 KB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC913 has 1 KB of on-chip Code memory.

INTERRUPTS

The P89LPC913 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC913 supports 10 interrupt sources: timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/ realtime clock, keyboard, comparators 1 and 2, and SPI.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

External interrupt inputs

The P89LPC913has a Keypad Interrupt function. This can be used as an external interrupt input. If enabled when the P89LPC913 is put into Power down or Idle mode, the keypad interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

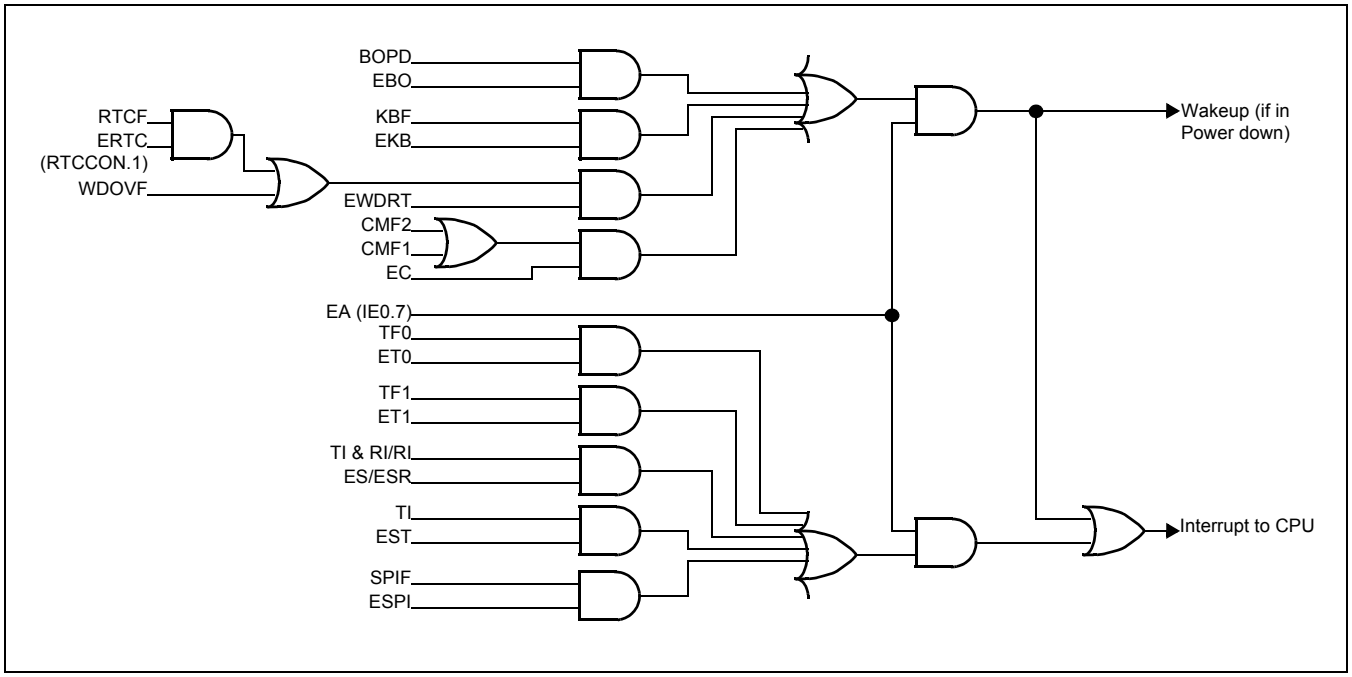


Figure 4: Interrupt sources, interrupt enables, and power-down wake-up sources

I/O PORTS

The P89LPC913 has 4 I/O ports: Port 0, Port 1, Port2, and Port 3. The exact number of I/O pins available depend upon the clock and reset options chosen:

Table 1: Number of I/O pins available.

Clock source	Reset option	Number of I/O pins
		14-pin package
On-chip oscillator or watchdog oscillator	No external reset(except during power-up)	12
	External $\overline{\text{RST}}$ pin supported	11
External clock input	No external reset(except during power-up)	11
	External $\overline{\text{RST}}$ pin supported	10
Low/medium/high speed oscillator (external crystal or resonator)	No external reset(except during power-up)	10
	External $\overline{\text{RST}}$ pin supported	9

Port configurations

All but one I/O port pin on the P89LPC913 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.

Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

P89LPC913 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

Open drain output configuration

The open drain output configuration turns off all pullups and only drives the pulldown transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit .

Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

Port 0 analog functions

The P89LPC913 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in the I/O Ports section.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, PT0AD bits defaults to ’0’s to enable digital functions.

Additional Port Features

After power-up, all pins are in Input-Only mode.After power-up, all I/O pins except P1.5, may be configured by software.

- Pin P1.5 is input only.
-

Every output on the P89LPC913 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to the section DC electrical characteristics for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

POWER MONITORING FUNCTIONS

The P89LPC913 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the operating voltage range for V_{DD} is 2.7 V-3.6 V, and the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{BO} (see DC Electrical Characteristics), and is negated when V_{DD} rises above V_{BO}. If brownout detection is disabled, the operating voltage range for V_{DD} is 2.4 V-3.6 V. If the P89LPC913 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see the DC Electrical Characteristics section of this datasheet for specifications.

Power-on Detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

POWER REDUCTION MODES

The P89LPC913 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC913 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (Note: Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock AND the RTC is enabled.

Total Power down Mode: This is the same as Power down Mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock AND the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power down.

Reset

The P1.5/$\overline{RST}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

NOTE: During a power-up sequence, the RPE selection is overidden and this pin will always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources :

- External reset pin (during power-up or if user configured via UCFG1);
- Power-on detect;
- Brownout detect;
- Watchdog Timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a ’0’ to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

TIMERS/COUNTERS 0 AND 1

The P89LPC913 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1.

In the "Timer" function, the register is incremented every machine cycle.

In the "Counter" function, the register of Timer 0 is incremented in response to a 1-to-0 transition at its external input pin, T0 . This external input is sampled once during every machine cycle.

Timer 0 has four operating modes (modes 0, 1, 2, and 3).

Timer 1 has four operating modes (modes 0, 1, 2, and 3). Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different.

Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

REAL-TIME CLOCK/SYSTEM TIMER

The LPC913 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all 0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time Clock and its associated SFRs to the default state.

UART

The LPC913 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The LPC913 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options.The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16

Mode 0
Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at 1/16 of the CPU clock frequency.

Mode 1
10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described later in section on "Baud rate generator and selection").

Mode 2
11 bits are transmitted (through TxD) or received (through RxD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

Mode 3
11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described later in section on "Baud rate generator and selection").

Baud rate generator and selection
The LPC91234 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 5). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is set. The independent Baud Rate Generator uses OSCCLK.

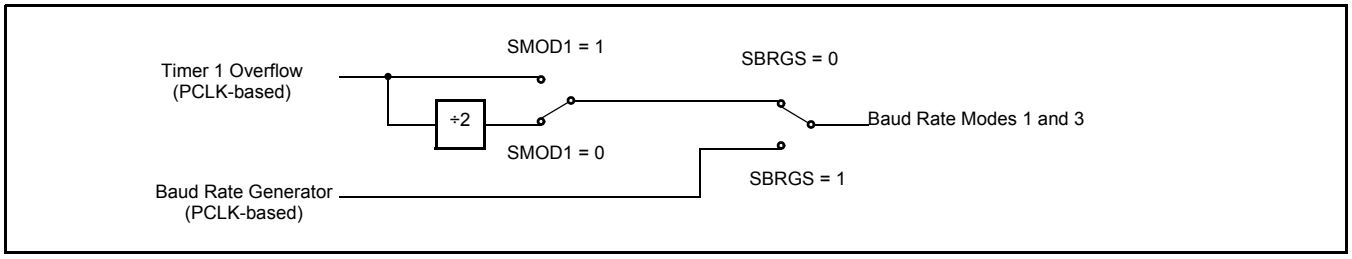


Figure 5: Baud rate sources for UART (Modes 1, 3)

Framing error
Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7-6) are set up when SMOD0 is ’0’.

Break detect
Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed low. The break detect can be used to reset the device.

Double buffering
The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e. SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

The 9th bit (Bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 MUST be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

SERIAL PERIPHERAL INTERFACE (SPI)

P89LPC913 provides another high-speed serial communication interface - the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation mode: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

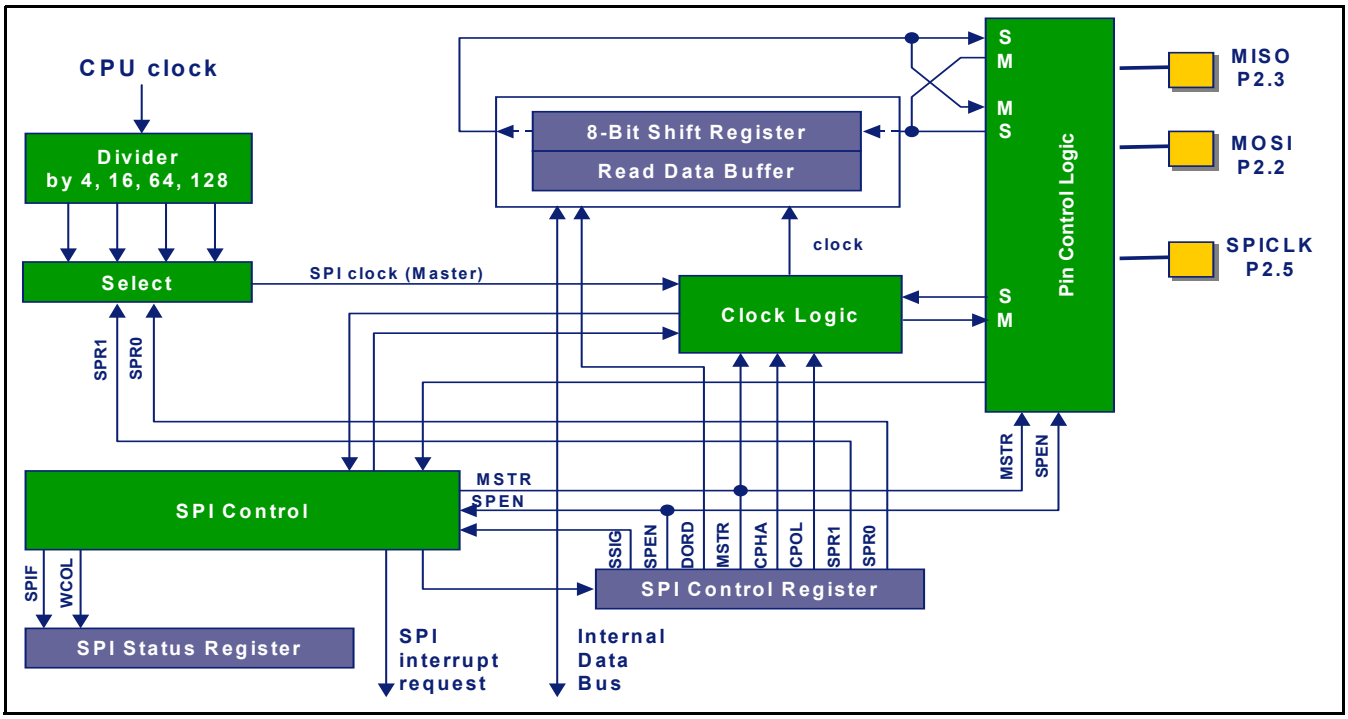


Figure 6: SPI block diagram

The SPI interface has three pins: SPICLK, MOSI, and MISO :

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e. SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.

- The 89LPC913 does not have the slave select pin, $\overline{SS}$. The SPI interface is set to Master mode and an I/O pin may be used to implement the $\overline{SS}$ function.

Typical connections are shown in Figures 7 - 8.

Typical SPI configurations

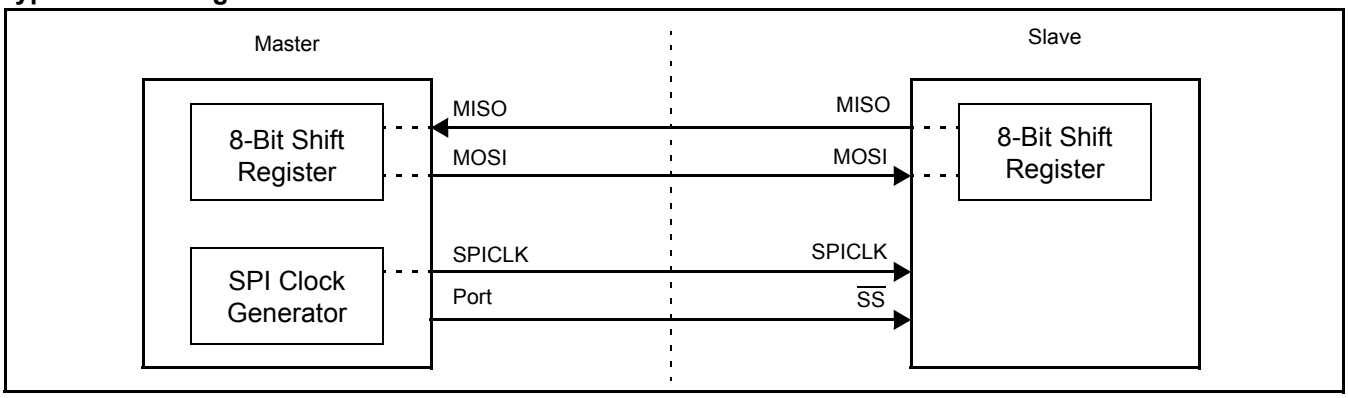


Figure 7: SPI single master single slave configuration

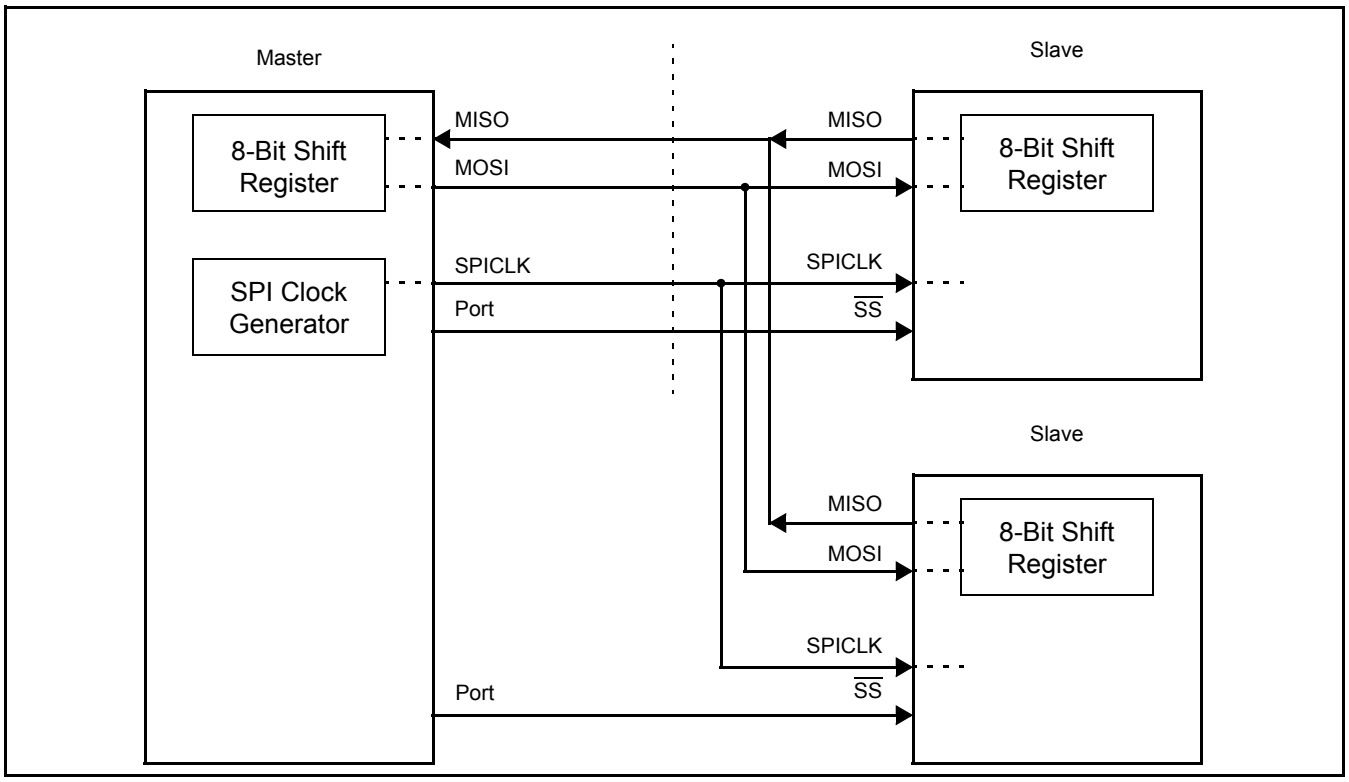


Figure 8: SPI single master multiple slaves configuration

ANALOG COMPARATORS

Two analog comparators are provided on the P89LPC913. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.Comparator 1 may be output to a port pin.

The overall connections to both comparators are shown in Figure 9. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{ref}, is 1.23 V ±10%.

Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

Possible conparator configurations are shown in Figure 10.

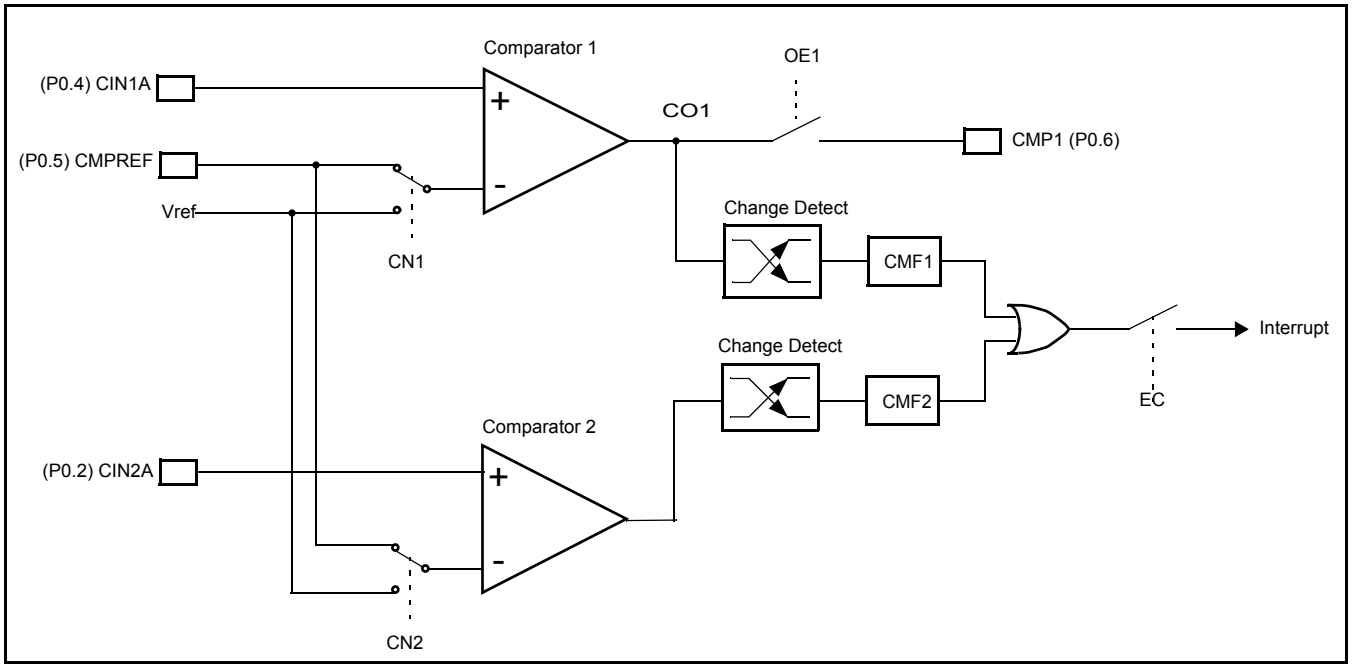


Figure 9: Comparator input and output connections

Comparators and Power Reduction Modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

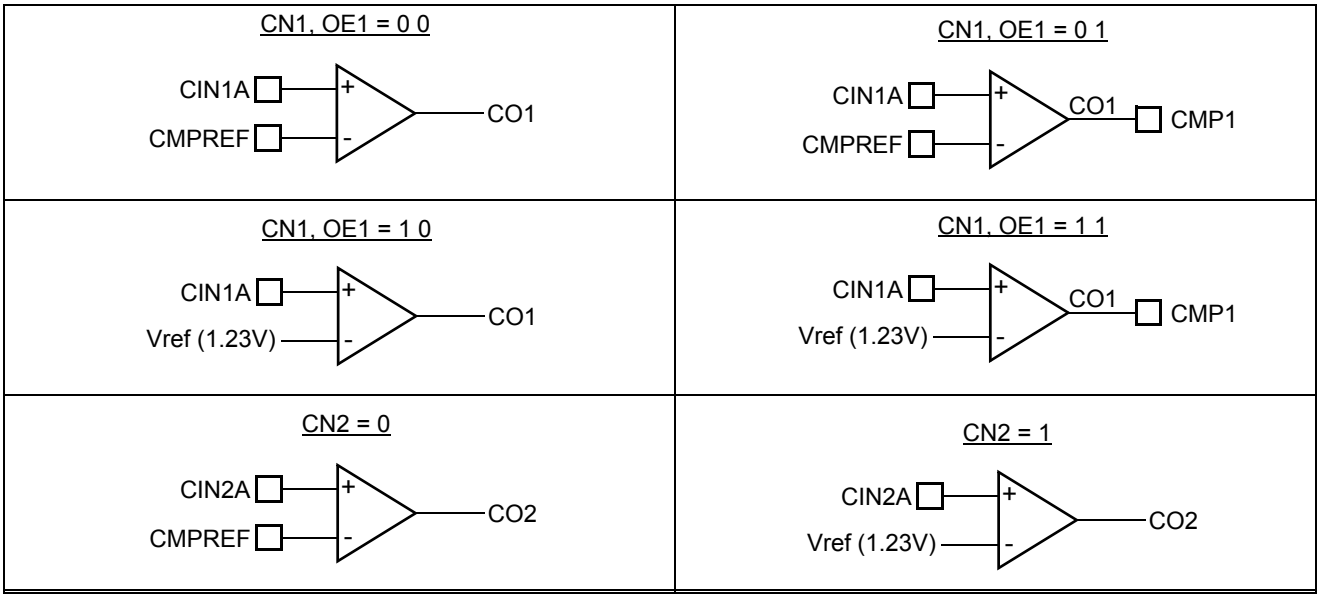


Figure 10: Comparator configurations

KEYPAD INTERRUPT (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

WATCHDOG TIMER

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 11 shows the watchdog timer in watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered down, the watchdog is disabled. The watchdog timer has a timeout period that ranges from a few µs to a few seconds. Please refer to the User's Manual for more details.

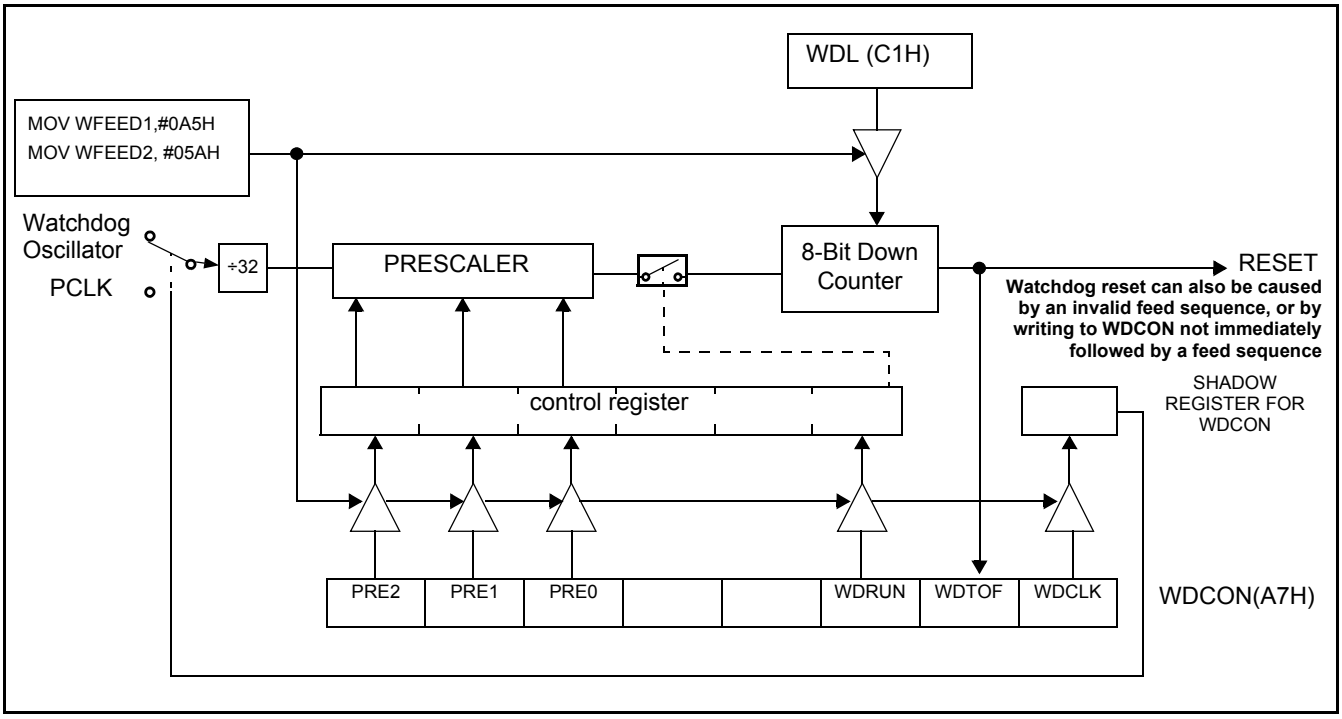


Figure 11: Watchdog timer in Watchdog mode (WDTE = 1)

ADDITIONAL FEATURES

Software Reset
The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

Dual Data Pointers
The dual Data Pointers (DPTR) provides two diferent Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

Flash program memory

General description
The P89LPC913 Flash memory provides in-circuit electrical erasure and programming. The Flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any Flash sector (256 bytes) or page (16 bytes). The Chip Erase operation will erase the entire program memory. In-Circuit Programming using standard commercial programmers is available. In addition, In-Application Programming (IAP) and byte erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC913 Flash reliably stores memory contents even after 10,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC913 uses VDD as the supply voltage to perform the Program/Erase algorithms.

Features –
- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ICP.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the Flash for each sector.
- 10,000 minimum erase/program cycles for each byte.
- 10-year minimum data retention.

Flash organization
The P89LPC913 program memory consists of four 256 byte sectors. Each sector can be further divided into 16-byte pages. In addition to sector erase, page erase, and byte erase, a 16-byte page register is included which allows from 1 to 16 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

Flash programming and erasing
Different methods of erasing or programming of the Flash are available. The Flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the In-Circuit Programming (ICP) mechanism. This ICP system provides for programming through a serial clock- serial data interface supported by commercially available EPROM programmers. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 1 KB of user code space.

In-circuit programming (ICP)
In-Circuit Programming is performed without removing the microcontroller from the system. The In-Circuit Programming facility consists of internal hardware resources to facilitate remote programming of the P89LPC913 through a two-wire serial interface. The Philips In-Circuit Programming facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the 89LPC913 User's Manual.

In-application programming (IAP)

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips In-Application Programming has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC913 User's Manual.

Using flash as data storage

The Flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

User configuration bytes

Some user-configurable features of the P89LPC913 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the User's Manual for additional details.

User sector security bytes

There are four User Sector Security Bytes each corresponding to one sector. Please see the User's Manual for additional details

Absolute maximum ratings

PARAMETER	RATING	UNIT
Temperature under bias	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Voltage on Xtal1, Xtal2 pin to V_{SS}	V_{DD}+0.5	V
Voltage on any other pin to V_{SS}	-0.5 to 5.5V	V
Maximum I_{OH} per I/O pin	8	mA
Maximum I_{OL} per I/O pin	20	mA
Maximum total I/O current	125	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC electrical characteristics

Vdd = 2.4 V to 3.6 V unless otherwise specified;
T_{amb} = 0 to +70°C for commercial, -40°C to +85°C for industrial, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
I_{DD}	Power supply current, operating	3.6V, 12 MHz [7]		15	25	mA
I_{ID}	Power supply current, Idle mode	3.6V, 12 MHz [7]		1	4	mA
I_{PD}	Power supply current, Power down mode, voltage comparators powered down	3.6 V [7]			tbd	µA
I_{PD1}	Power supply current, Total Power down mode	3.6 V [7]		1	5	µA
V_{DDR}	Vdd rise time				2	mV/µs
V_{DDF}	Vdd fall time				50	mV/µs
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Negative going threshold (Schmitt input)		$0.22V_{DD}$	$0.4V_{DD}$		V
V_{IH}	Positive going threshold (Schmitt input)			$0.6V_{DD}$	$0.7V_{DD}$	V
HYS	Hysteresis voltage			$0.2V_{DD}$		V
V_{OL}	Output low voltage all ports	I_{OL} = 20mA, V_{DD} = 2.4 V - 5.5 V		0.6	1.0	V
		I_{OL} = 10mA, V_{DD} = 2.4 V - 5.5 V		0.3	0.5	V
		I_{OL} = 3.2mA, V_{DD} = 2.4 V - 5.5 V		0.2	0.3	V
V_{OH}	Output high voltage, all ports	I_{OH} = -8mA, V_{DD} = 2.4 V - 5.5 V, push-pull mode	V_{DD}-TBD			V
		I_{OH} = -3.2mA,V_{DD} = 2.4 V - 5.5 V, push-pull mode	V_{DD}-0.7	V_{DD}-0.4		V
		I_{OH} = -20µA, V_{DD} = 2.4 V, quasi-bidirectional mode	V_{DD}-0.3	V_{DD}-0.2		
C_{IO}	Input/Output pin capacitance [6]				15	pF
I_{IL}	Logical 0 input current, all ports [5]	V_{IN} = 0.4 V			-50	µA
I_{LI}	Input leakage current, all ports [4]	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{TL}	Logical 1 to 0 transition current, all ports [2, 3]	V_{IN} = 1.5 V at V_{DD} = 3.6 V	-30		-250	µA
R_{RST}	Internal reset pullup resistor		11		24	kΩ
V_{BO}	Brownout trip voltage, BOV = 1, BOPD = 0	2.4 V < V_{DD} < 3.6 V	2.40		2.70	V
V_{REF}	Bandgap reference voltage		1.11	1.23	1.34	V
t_C (V_{REF})	Bandgap temperature coefficient			10	20	ppm/°C

Notes:
1. Typical ratings are not guaranteed. The values listed are ar room temperature, 3 V.
2. Ports in quasi-bidirectional mode with weak pullup (applies to all port pins with pullups).
3. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
4. Measured with port in high impedance mode.
5. Measured with port in quasi-bidirectional mode.
6. Pin capacitance is characterized but not tested.
7. I_{DD} , I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer.

AC electrical characteristics

T_{amb} = 0 to +70°C for commercial, -40°C to +85°C for industrial, unless otherwise specified.[2]

SYMBOL	FIGURE (S)	PARAMETER	Variable Clock		f_{OSC}=12MHz		UNIT
			MIN	MAX	MIN	MAX	
f_{RCOSC}		Internal RC oscillator frequency	7.189	7.557	7.189	7.557	MHz
f_{WDOSC}		Internal watchdog oscillator frequency	280	480	280	480	KHz
f_{OSC}		Oscillator frequency	0	12			MHz
t_{CLCL}	13	CLock cycle	83				ns
f_{CLKLP}		CLKLP active frequency	0	4			MHz
Glitch Filter							
		P1.5($\overline{RST}$) pin glitch rejection		50		50	ns
		P1.5($\overline{RST}$) pin signal acceptance	125		125		ns
		Glitch rejection - any pin except P1.5($\overline{RST}$)		15		15	ns
		Signal acceptance - any pin except P1.5($\overline{RST}$)	50		50		ns
External Clock							
t_{CHCX}	13	High time	33	t_{CLCL}-t_{CLCX}	33		ns
t_{CLCX}	13	Low time	33	t_{CLCL}-t_{CHCX}	33		ns
t_{CLCH}	13	Rise time		8		8	ns
t_{CHCL}	13	Fall Time		8		8	ns
Shift Register(UART mode 0)							
t_{XLXL}		Serial port clock cycle time	16 t_{CLCL}		1333		ns
t_{QVXH}		Output data setup to clock rising edge	13 t_{CLCL}		1083		ns
t_{XHQX}		Output data hold after clock rising edge		t_{CLCL}+20		103	ns
t_{XHDX}		Input data hold after clock rising edge		0		0	ns
t_{DVXH}		Input data valid to clock rising edge	150		150		ns

Notes:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified;
T_{amb} = 0 to +70°C for commercial, -40°C to +85°C for industrial, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN		MAX	
V_{IO}	Offset voltage comparator inputs				±20	mV
V_{CR}	Common mode range comparator inputs		0		V_{DD}-0.3	V
CMRR	Common mode rejection ratio [1]				-50	dB
	Response time			250	500	ns
	Comparator enable to output valid				10	µs
I_{IL}	Input leakage current, comparator	$0 < V_{IN} < V_{DD}$			±10	µA

Notes:
1. This parameter is characterized, but not tested in production.

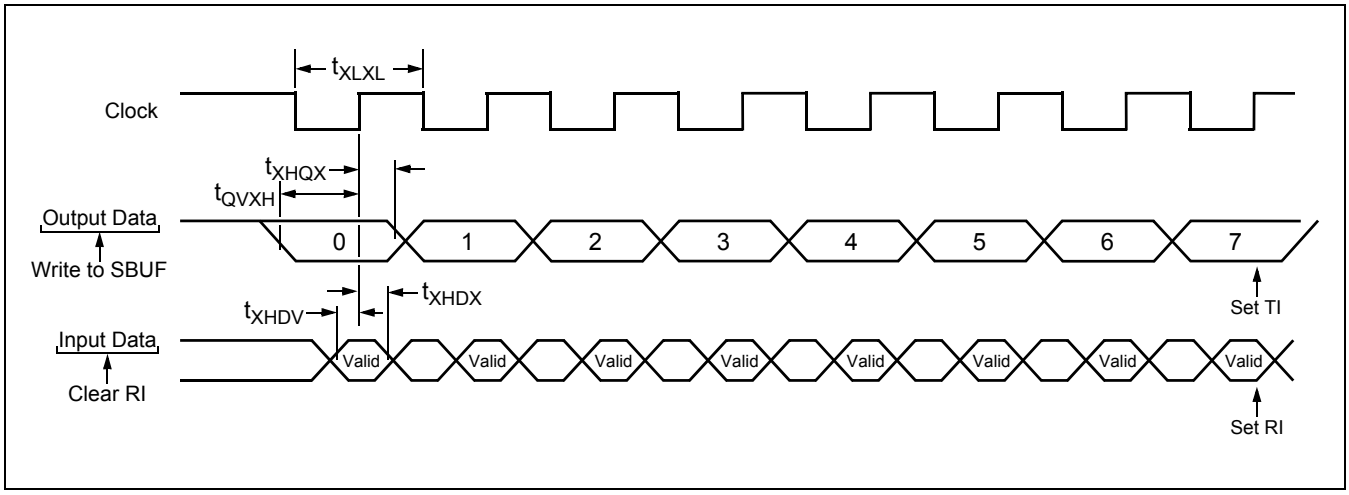


Figure 12: Shift Register Mode Timing

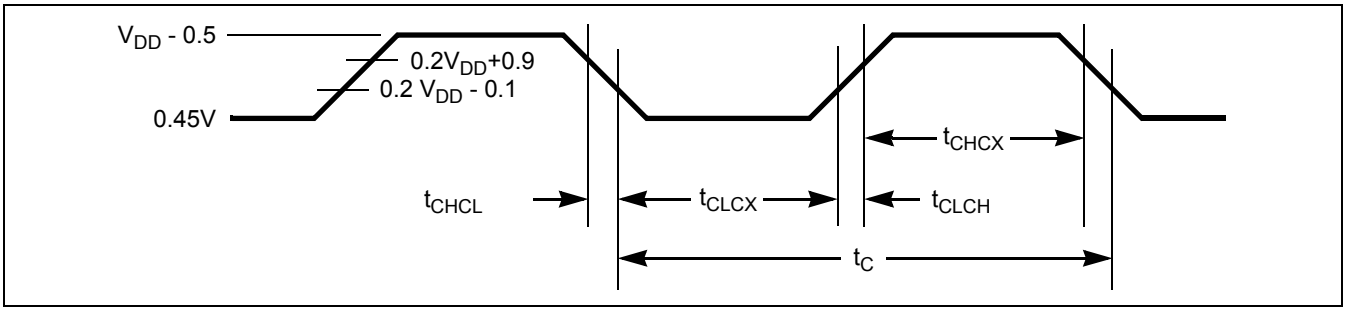


Figure 13: External Clock Timing